Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended). A configuration, comprising:

at least one first device;

a cross bar;

at least one second device connected to said at least one first device through said cross bar, said at least one first device accessing said at least one second device through said cross bar to at least one of read data from said at least one second device and write data to said at least one second device;

a first multiplexer associated with each of said at least one first device, ~~said~~ each first multiplexer ~~associated with each of said at least one first device~~ having input connections connecting directly or via a pipeline stage to all of said at least one second device through read data buses and an output connection connecting to the ~~respective~~ associated one of said at least one first device through a read data bus;

an arbiter associated with each of said at least one second device, ~~said~~ each arbiter having input connections connecting directly or via a pipeline stage to all of said at least one first device through address buses and an output connection connecting to the ~~respective~~ associated one of said at least one second device through an address bus; and

a second multiplexer associated with each of said at least one second device, ~~said~~ each second multiplexer ~~associated with each of said at least one second device~~ having input connections connecting directly or via a pipeline stage to all of said at least one first device through write data buses and an output connection connecting to the ~~respective~~ associated one of said at least one second device through a write data bus;

wherein said pipeline stage is not one of said first multiplexers, one of said arbiters, or one of said second multiplexers.

Claim 2 (previously presented). The configuration according to claim 1, further comprising:

at least one first address bus;

at least one second address bus;

at least one first read data bus;

at least one second read data bus;

at least one first write data bus;

at least one second write data bus;

each of said at least one first device and said cross bar being connected to one another through a respective one of said at least one first address bus, a respective one of said at least one first read data bus, and a respective one of said at least one first write data bus; and

each of said at least one second device and said cross bar being connected to one another through a respective one of said at least one second address bus, a respective one of said at least one second read data bus, and a respective one of said at least one second write data bus.

Claim 3 (previously presented). The configuration according to claim 2, wherein one of said at least one first device

sends a request signal to said cross bar when said first device wishes to make a read access to one of said at least one second device.

Claim 4 (previously presented). The configuration according to claim 3, wherein said first device sends an address to said cross bar at the same time as the request signal, said address specifying a second device and a point within said second device from which data should be read.

Claim 5 (cancelled).

Claim 6 (previously presented). The configuration according to claim 4, wherein said first device transmits the request signal and the address to said cross bar through a respective first address bus.

Claim 7 (original). The configuration according to claim 3, wherein said cross bar confirms the read access request by transmission of a grant signal to said first device.

Claim 8 (previously presented). The configuration according to claim 7, wherein said cross bar transmits the grant signal to said first device through a respective first address bus.

Claim 9 (previously presented). The configuration according to claim 4, wherein said cross bar passes on at least a portion of the address supplied to said cross bar through a respective second address bus to said second device from which data should be read.

Claim 10 (original). The configuration according to claim 9, wherein said second device emits to said cross bar the data stored at the address supplied to said second device.

Claim 11 (original). The configuration according to claim 10, wherein said second device emits the ready signal to said cross bar at the same time that said second device emits the data that has been read.

Claim 12 (previously presented). The configuration according to claim 11, wherein said second device transmits the data that has been read and the ready signal to said cross bar through a respective second read data bus.

Claim 13 (previously presented). The configuration according to claim 12, wherein said cross bar passes on the data supplied thereto and the ready signal supplied thereto through a respective first read data bus to said first device.

Claim 14 (previously presented). The configuration according to claim 2, wherein one of said at least one first device sends a request signal to said cross bar when said first device wishes to make a write access to one of said at least one second device.

Claim 15 (previously presented). The configuration according to claim 14, wherein said first device sends an address to said cross bar at the same time as the request signal, the address specifying a second device and a point within said second device to which data should be written.

Claim 16 (previously presented). The configuration according to claim 15, wherein said first device transmits the request signal and the address to said cross bar through a respective first address bus.

Claim 17 (original). The configuration according to claim 14, wherein said cross bar confirms the write access request from said first device by transmitting a grant signal to said first device.

Claim 18 (previously presented). The configuration according to claim 17, wherein said cross bar transmits the grant signal to said first device through a respective first address bus.

Claim 19 (previously presented). The configuration according to claim 15, wherein said cross bar passes on at least a portion of the address supplied to said cross bar through ~~said~~ a respective second address bus to said second device to which data should be written.

Claim 20 (original). The configuration according to claim 19, wherein said second device emits a ready signal to said cross bar when said second device is ready to receive the data to be stored in said second device.

Claim 21 (previously presented). The configuration according to claim 20, wherein said second device transmits the ready signal to said cross bar through a respective second read data bus.

Claim 22 (previously presented). The configuration according to claim 21, wherein said cross bar passes on the ready signal to said first device through a respective first read data bus.

Claim 23 (original). The configuration according to claim 22, wherein said first device emits to said cross bar the data to be written to said second device.

Claim 24 (original). The configuration according to claim 23, wherein said first device emits the data valid signal to said cross bar at the same time that said first device emits the data to be written to said second device.

Claim 25 (previously presented). The configuration according to claim 24, wherein a respective first write data bus transmits the data emitted from said first device and the data valid signal emitted from said first device to said cross bar.

Claim 26 (previously presented). The configuration according to claim 25, wherein said cross bar passes on the data and the data valid signal supplied to said cross bar to said second device through a respective second write data bus.

Claim 27 (currently amended). A method for at least one of reading and writing data, which comprises:

connecting at least one second device to at least one first device through a cross bar;

accessing one of the at least one ~~the~~ second device with one of the at least one first device through the cross bar for at least one of reading and writing data;

associating a first multiplexer with each of the at least one first device, ~~the~~ each first multiplexer ~~associated with each of the at least one first device~~ having input connections connecting directly or via a pipeline stage to all of the at least one second device through read data buses and an output connection connecting to the ~~respective~~ associated one of the at least one first device through a read data bus;

associating an arbiter with each of the at least one second device, ~~the~~ each arbiter having input connections connecting directly or via a pipeline stage to all of the at least one first device through address buses and an output connection connecting to the ~~respective~~ associated one of the at least one second device through an address bus;

associating a second multiplexer with each of the at least one second device, ~~the~~ each second multiplexer ~~associated with each of the at least one second device~~ having input connections connecting directly or via a pipeline stage to all of the at least one first device through write data buses and an output connection connecting to the ~~respective~~ associated one of the at least one second device through a write data bus~~;~~

~~when a read access to the second device occurs, reading the data emitted from the second device with the first device when the first device receives a ready signal produced by the second device and supplied to the first device through the cross bar; and~~

~~when a write access from the first device to the second device occurs:~~

~~emitting, from the first device, the data to be written to the second device when the first device receives a ready signal produced by the second device and supplied to the first device through the cross bar; and~~

~~reading the data emitted from the first device with the second device when the second device receives a data valid signal produced by the first device and supplied to the second device through the cross bar~~

wherein the pipeline stage is not one of the first multiplexers, one of the arbiters, or one of the second multiplexers.

Claim 28 (cancelled).